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10/689,979	10/20/2003	Joseph Smart	2867-207	3803

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CK

Office Action Summary	Application No.	Applicant(s)	
	10/689,979	SMART ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In paragraph [0021], lines 16-17 of Specification should be completed by file out the blank. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of "the GaN termination layer is further a **reproducible termination layer**, thereby increasing effectiveness of passivation", as recited in claims 6 and 14, is unclear as to what it means "**reproducible termination layer**".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5, 9, 11-13, 17-19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Teraguchi et al. (U.S. 6,177,685).

Regarding claims 1-2 and 11, Teraguchi (figures 1 and 7) discloses a high voltage gallium nitride (GaN) transistor structure (column 1, lines 5-19) comprising:

a) a substrate 1;

b) a plurality of epitaxial layers (column 3, lines 39-42) deposited on the substrate and comprising:

i) a transitional layer (not shown, see column 8, lines 8-11) deposited above the substrate;

ii) a sub-buffer (AlN) layer 2/32 (column 3, line 30 or column 7, lines 3-5) deposited above the transitional layer and adapted to prevent electrons from entering the transitional layer and the substrate during high voltage operation (column 7, lines 35-41); and

iii) a GaN buffer layer 3/33 deposited above the sub-buffer layer 2 (column 3, line 31 or column 7, lines 5-7); and

c) electrical contacts 7/8 deposited on the plurality of epitaxial layers, thereby forming a high electron mobility transistor (column 7, lines 10-12).

Regarding claims 3 and 19, Teraguchi (figures 1 and 7) discloses the plurality of epitaxial layers further comprise an Schottky layer 5 deposited above the GaN buffer layer 3.

Regarding claim 5, Teraguchi (figures 1 and 7) discloses wherein the plurality of epitaxial layers further comprise a GaN termination layer 6 (column 3, line 37) deposited above the Schottky layer 5 and adapted to protect the Schottky layer from surface reactions.

Regarding claims 9 and 21, Teraguchi (figures 1 and 7) discloses the contacts comprise a source contact 8, a gate contact 7, and a drain contact 8, further wherein the source, gate, and drain contacts are metallic (column 5, lines 5-6).

Regarding claim 12, Teraguchi (figure 10) discloses a high voltage gallium nitride (GaN) transistor structure (column 1, lines 5-19) comprising: a substrate 301; a transitional layer (not shown, see column 8, lines 8-11) deposited above the substrate; a sub-buffer layer 302 deposited above the transitional layer; a GaN buffer layer 303 deposited above the sub-buffer layer 302 (column 1, lines 50-59); an aluminum nitride Schottky layer 304 deposited on the gallium nitride buffer layer 303; and a GaN termination layer 305 deposited on the Schottky layer 304 (column 1, lines 50-59).

Regarding claim 13, Teraguchi (figures 1 and 7) discloses a gallium nitride (GaN) transistor structure (column 1, lines 5-19) comprising:

a) a substrate 1;

b) a plurality of structural epitaxial layers deposited on the substrate and includes a GaN buffer layer 3 (column 3, line 31 or column 7, lines 5-7);

c) a GaN termination layer 6 (column 3, line 37) deposited on the plurality of structural epitaxial layers and adapted to protect the plurality of structural epitaxial layers from surface reactions; and

d) electrical contacts deposited on the GaN termination layer, thereby forming a high electron mobility transistor (column 7, lines 10-12).

Regarding claim 17, Teraguchi (figures 1 and 7) discloses a plurality of structural epitaxial layers further comprise a transitional layer deposited above the substrate (column 8, lines 8-11).

Regarding claim 18, Teraguchi (figures 1 and 7) discloses wherein a GaN buffer layer 3 (column 3, line 31 or column 7, lines 5-7) deposited above the transitional layer.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 7-13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (U.S. 6,624,452) in view of Teraguchi et al. (U.S. 6,177,685).

Regarding claims 1-2 and 11, Yu (figure 1) discloses a high voltage gallium nitride (GaN) transistor structure (column 2, line 62) comprising:

a substrate 12; a plurality of epitaxial layers (column 4, lines 34-42) deposited on the substrate and comprising: a transitional (or nucleation) layer 14 (column 2, line 64) deposited above the substrate; a GaN buffer layer 16 deposited above the substrate (column 3, lines 32-33); and electrical contacts deposited on the plurality of epitaxial layers, thereby forming a high electron mobility transistor (column 2, lines 1-3).

Yu does not teach more than one buffer layer deposited above the transitional layer.

However, Teraguchi (figure 1) teaches an AlN sub-buffer layer 2 and GaN buffer layer 3 (column 3, lines 30-31) deposited above the transitional layer and adapted to prevent electrons from entering the transitional layer and the substrate during high voltage operation (column 7, lines 35-41). Furthermore, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. **St. Regis Paper Co. v. Bemis Co., 193 USPQ 8**. Therefore, it would have been obvious to form one or more buffer layers in Yu's device because they both provide the same result of preventing carriers from flowing into the substrate during high voltage operation, as taught by Teraguchi (column 7, lines 35-41).

Regarding claims 3-4 and 19-20, Yu (figure 1) discloses the plurality of epitaxial layers further comprise a Schottky layer 18 deposited above the GaN buffer layer 16 wherein the Schottky layer is essentially aluminum gallium nitride (column 4, lines 15-16).

Regarding claim 5, Yu (figure 1) discloses wherein the plurality of epitaxial layers further comprise a GaN termination layer 22 (column 3, line 67) deposited above the Schottky layer 18 and adapted to protect the Schottky layer from surface reactions (column 4, lines 1-14).

Regarding claims 7-8 and 15-16, Yu (figure 1) discloses the GaN termination is approximately 10 nanometers (nm) thick that is sufficiently thin to allow electron to tunnel through the GaN termination layer.

Yu does not teach the GaN termination is approximately 1-2 nanometers (nm) thick. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the GaN termination that is approximately 1-2 nanometers (nm) thick in Yu's device because the thickness of the GaN termination layer is not critical, it can be optimized depending upon the voltage applied to the device. It has been held where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. *Titanium Metals Corporation of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed, Cir. 1985).*

Regarding claims 9 and 21, Yu (figure 1) discloses the contacts comprise a source contact 24, a gate contact 28, and a drain contact 26, further wherein the source, gate, and drain contacts are metallic (column 3, lines 27-31).

Regarding claim 10, Yu does not disclose a source-drain breakdown voltage which is at least 100 volts. However, it would have been obvious to have a gallium nitride based HFET of Yu for operating at a source-drain breakdown voltage at least 100 volts because as is well known, HFET is a high power transistor which operates at a high voltage level.

Regarding claim 12, Yu (figure 1) discloses wherein the plurality of epitaxial layers further comprise: an aluminum nitride Schottky layer 18 deposited on the gallium nitride buffer layer 16; and a GaN termination layer 22 deposited on the Schottky layer 18 (column 3, lines 63-67).

Regarding claim 13, Yu (figure 1) discloses a gallium nitride (GaN) transistor structure (column 2, line 62) comprising:

a) a substrate 12;

b) a plurality of structural epitaxial layers deposited on the substrate and includes a GaN buffer layer 16 (column 3, lines 32-33);

c) a GaN termination layer 6 (column 3, lines 36-37) deposited on the plurality of structural epitaxial layers and adapted to protect the plurality of structural epitaxial layers from surface reactions; and

d) electrical contacts (24,26,28) deposited on the GaN termination layer, thereby forming a high electron mobility transistor.

Regarding claim 17, Yu (figure 1) discloses a plurality of structural epitaxial layers further comprise a transitional layer 14 deposited above the substrate (column 2, line 64).

Regarding claim 18, Yu (figure 1) discloses wherein a GaN buffer layer 16 deposited above the transitional layer 14 (column 2, lines 62-65).

8. Claims 1-5, 7-13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Micovic et al. (U.S. Pub. 2003/0218183) in view of Teraguchi et al. (U.S. 6,177,685).

Regarding claims 1-2 and 11, Micovic (figure 18a) discloses a high voltage gallium nitride (GaN) transistor structure comprising:

a substrate 1800; a plurality of epitaxial layers deposited on the substrate and comprising: a transitional (or nucleation) layer 1802 deposited above the substrate; a GaN buffer layer 1804 deposited above the substrate; and electrical contacts deposited on the plurality of epitaxial layers, thereby forming a high electron mobility transistor (see figure 13, paragraph [0072]).

Micovic does not teach more than one buffer layer deposited above the transitional layer.

However, Teraguchi (figure 1) teaches an AlN sub-buffer layer 2 and GaN buffer layer 3 (column 3, lines 30-31) deposited above the transitional layer and adapted to prevent electrons from entering the transitional layer and the substrate during high

voltage operation (column 7, lines 35-41). Furthermore, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. **St. Regis Paper Co. v. Bemis Co., 193 USPQ 8**. Therefore, it would have been obvious to form one or more buffer layers in Micovic's device because they both provide the same result of preventing carriers from flowing into the substrate during high voltage operation, as taught by Teraguchi (column 7, lines 35-41).

Regarding claims 3-4 and 19-20, Micovic (figure 18a) discloses the plurality of epitaxial layers further comprise a Schottky layer 1808 deposited above the GaN buffer layer 16804 wherein the Schottky layer is essentially aluminum gallium nitride.

Regarding claim 5, Micovic (figure 18a) discloses wherein the plurality of epitaxial layers further comprise a GaN termination layer 1810b deposited above the Schottky layer 1808 and adapted to protect the Schottky layer from surface reactions (see paragraphs from [0089] to [0091]).

Regarding claims 7-8 and 15-16, Micovic (figures 13 and 18a) discloses the GaN termination layer 1112 is approximately 5 nanometers (nm) thick (see figure 11, paragraph [0067]) that is sufficiently thin to allow electron to tunnel through the GaN termination layer.

Micovic does not teach the GaN termination is approximately 1-2 nanometers (nm) thick. It would have been obvious to one having ordinary skill in the art at the time

of the invention was made to form the GaN termination that is approximately 1-2 nanometers (nm) thick in Micovic's device, since it has been held where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. *Titanium Metals Corporation of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed, Cir. 1985).*

Regarding claims 9 and 21, Micovic (figure 13) discloses the contacts comprise a source contact 1202, a gate contact 1308, and a drain contact 1204, further wherein the source, gate, and drain contacts are metallic (see paragraph [0070]).

Regarding claim 10, Micovic does not disclose a source-drain breakdown voltage which is at least 100 volts. However, it would have been obvious to have a gallium nitride based HFET of Yu for operating at a source-drain breakdown voltage at least 100 volts because as is well known, HFET is a high electron mobility transistor which operates at a high voltage level.

Regarding claim 12, Micovic (figure 18a) discloses wherein the plurality of epitaxial layers further comprise: an aluminum nitride Schottky layer 1808 deposited on the gallium nitride buffer layer 1804; and a GaN termination layer 1810b deposited on the Schottky layer 1808.

Regarding claim 13, Micovic (figures 13 and 18a) discloses a gallium nitride (GaN) transistor structure comprising:

a) a substrate 1800;

b) a plurality of structural epitaxial layers deposited on the substrate and includes a GaN buffer layer 1804;

c) a GaN termination layer 1810b deposited on the plurality of structural epitaxial layers and adapted to protect the plurality of structural epitaxial layers from surface reactions; and

d) electrical contacts deposited on the GaN termination layer, thereby forming a high electron mobility transistor (see paragraphs from [0089] to [0091]).

Regarding claim 17, Micovic (figures 18a) discloses a plurality of structural epitaxial layers further comprise a transitional layer 1802 deposited above the substrate.

Regarding claim 18, Micovic (figures 18a) discloses wherein a GaN buffer layer 1804 deposited above the transitional layer 1802.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
January 7, 2005.

PHAT X. CAO
PRIMARY EXAMINER